Advanced Analog Integrated Circuits

Switched Capacitor Gain Stages

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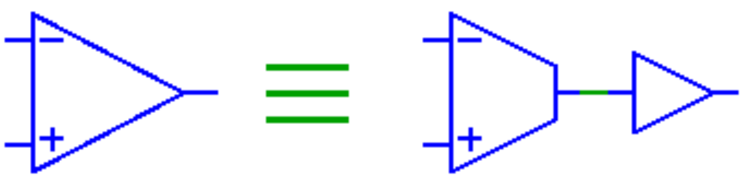
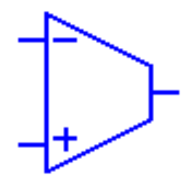
OpAmp versus OTA

OpAmp



- Low output resistance (voltage source)
- Buffer benefits from high g_m
- Gain independent of R_L
- Often preferable with BJT

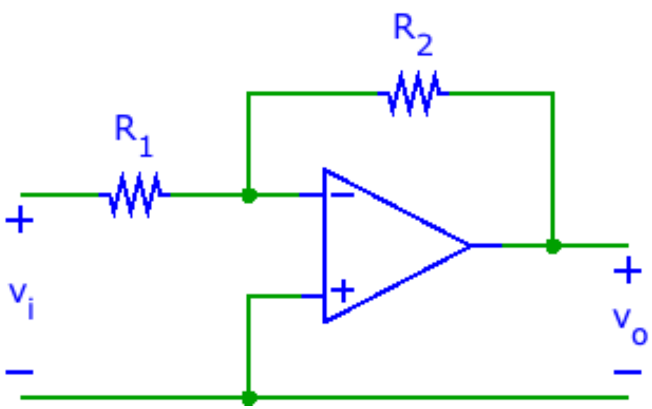
OTA



- High output resistance (current source)
- No buffer
- Can't "drive" low R_L
- Preferable with MOS

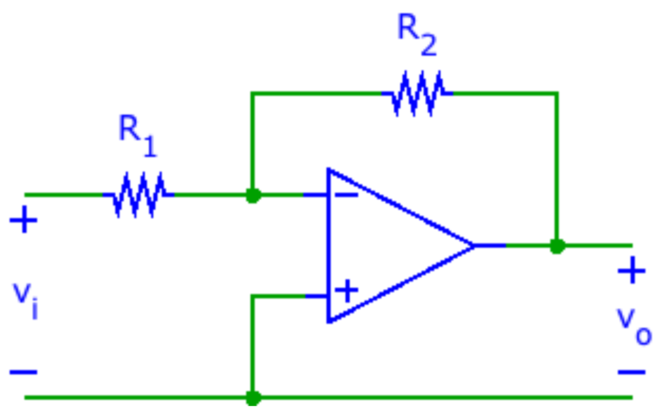
Gain Stages

Resistive Feedback

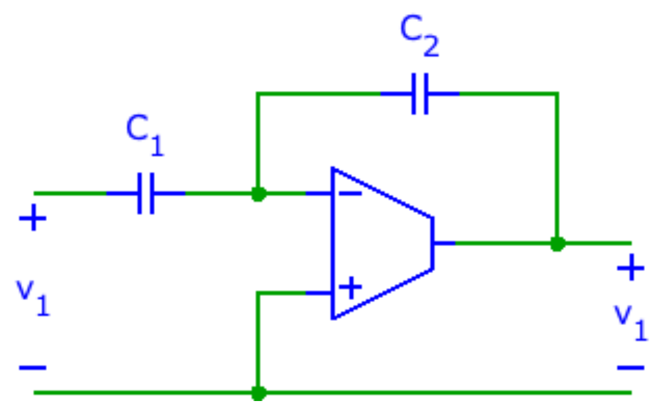


Gain Stages

Resistive Feedback



Capacitive Feedback



Transconductor Choices

BJT **MOS**

Aside: MOS Voltage Buffers

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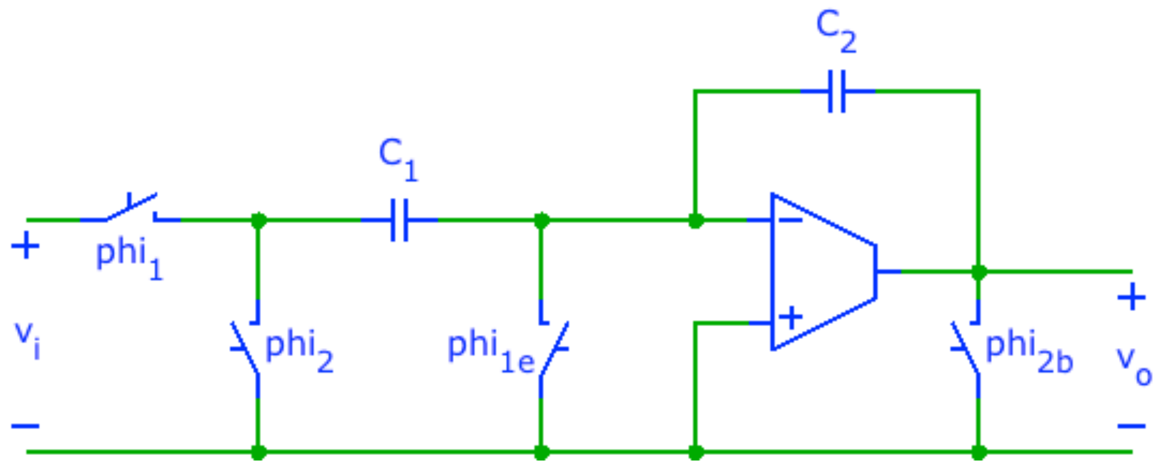
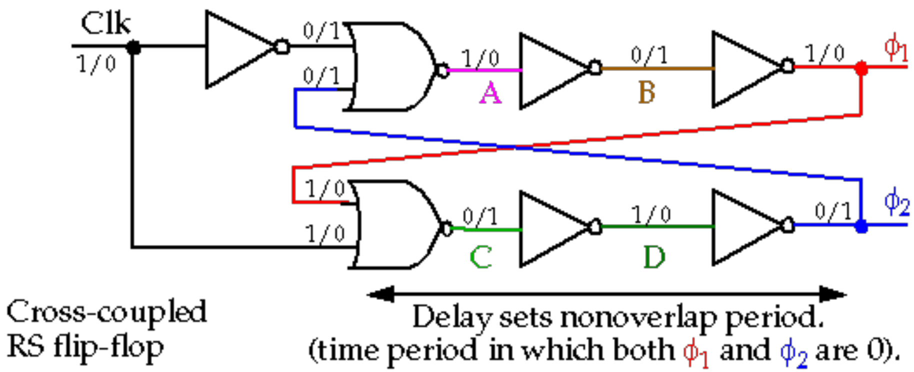
SC Gain Stage

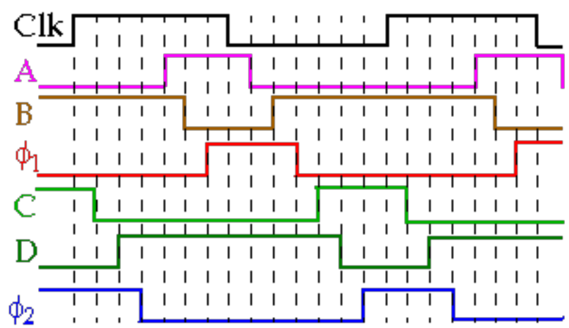


Switches controlled from non-overlapping 2-phase clock:

Note: ***important*** details of clocks and switches will be discussed later.

Multiphase Clock Generators





http://ece-research.unm.edu/jimp/vlsi/slides/chap5_2-34.gif

Spectre:

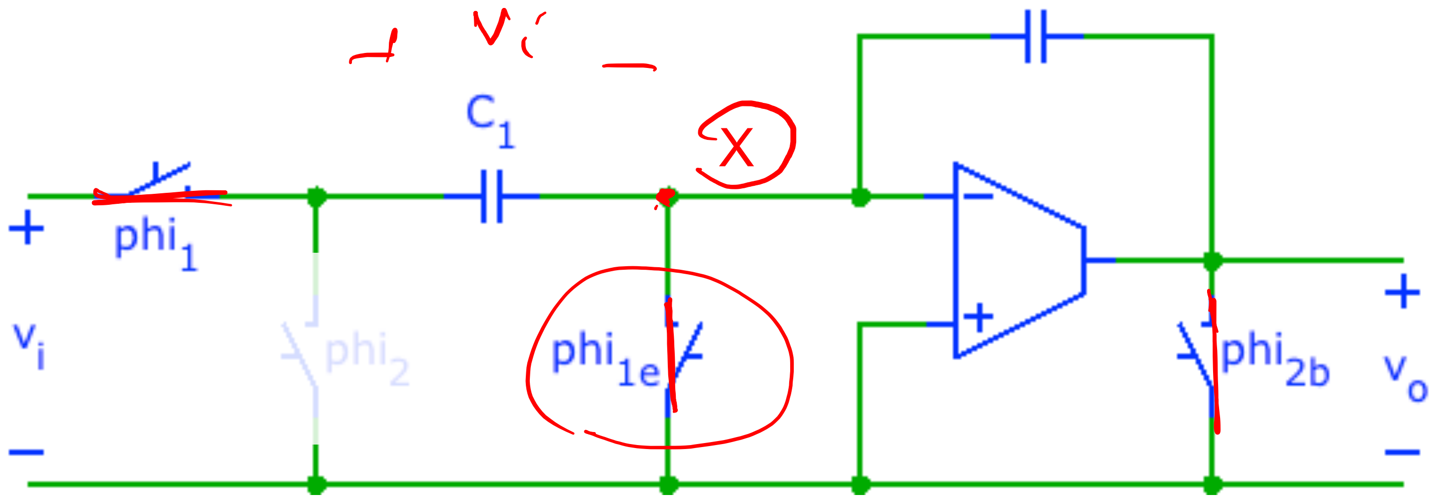
```
  phi1 (vphi1 0) vsource type=pulse val0=0 val1=1.8
+ period=1/fs width=0.45/fs delay=0.01/fs
```

Phase 1

$Q_1 = -V_i \cdot C_1$

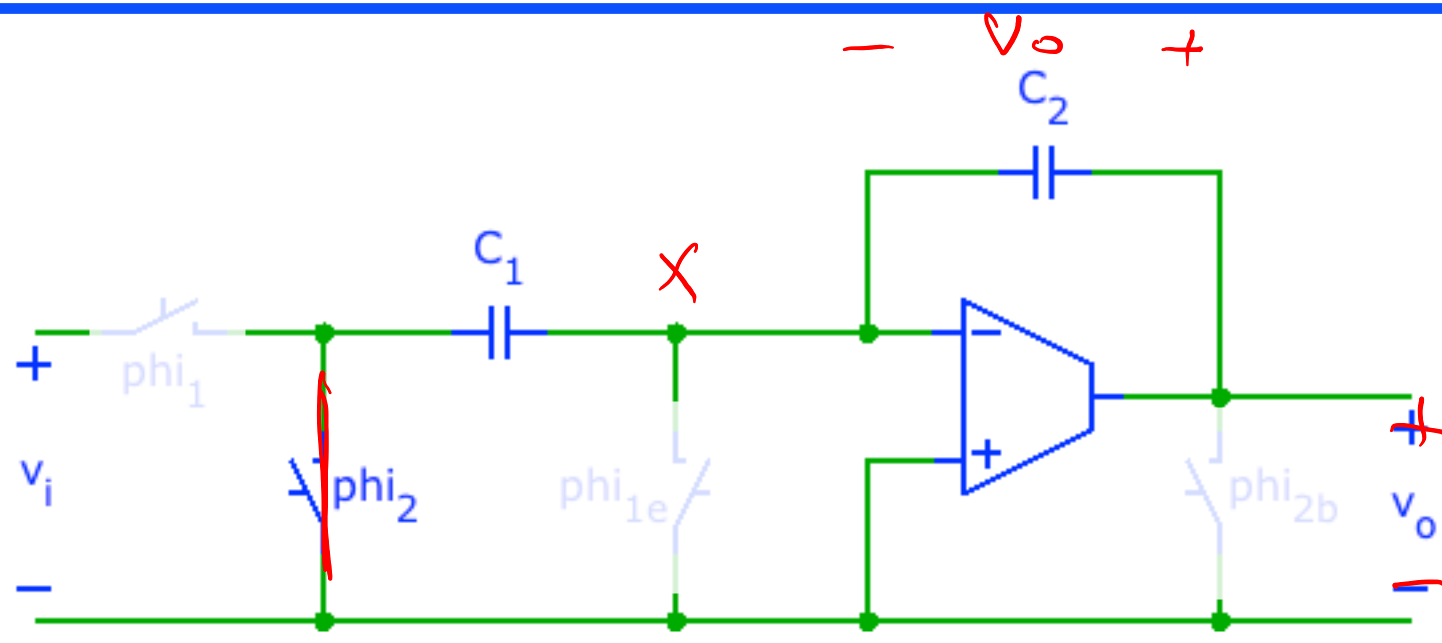
$Q_2 = \emptyset$

$+ \; V_i \; -$



$$Q_{x1} = -V_i C_1 + 0 \cdot C_2$$

Phase 2



$$Q_{x2} = 0 \cdot C_1 = v_o \cdot C_2$$

$$= Q_{x1}$$

Charge Conservation

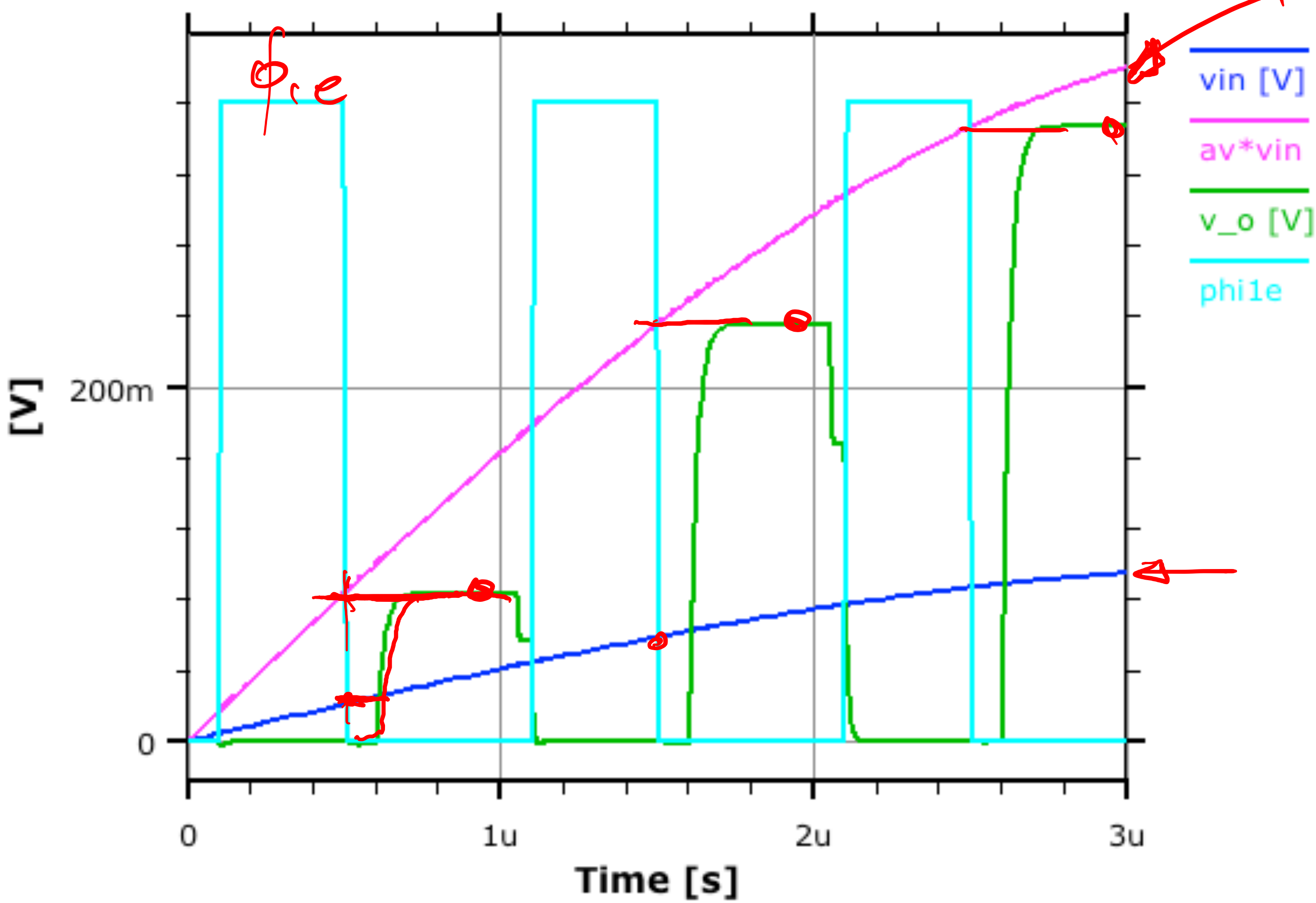
Since no charge escapes when switching from phase 1 to phase 2:

$$Q_{x1} = Q_{x2}$$

$$\therefore \quad \frac{V_o}{V_i} = + \frac{C_1}{C_2}$$

Transient Analysis

$V_i \cdot \left(a_v = \frac{C_1}{C_2}\right)$



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Time Invariant Circuits

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Switched Capacitor Circuits

- Signals valid @ discrete times (clock) f_s
- Spectrum: 0 ... $f_s/2$
- SC: OTAs, switches, caps
- SC circuit apps
  - → amp, (non) inverting
  - → integrators → filters ← 245C
  - → 1/f, offset 240B

Time Invariant and Linear

- SC gain → linear

  $v_o \propto v_i$

- Time variant

- ac ?

  periodic:

  op → pss

  ac → pac

Periodic ac Simulation (Spectre)

- Perform first a "periodic operating point analysis":

```
pss1 pss fund=fs maxacfreq=20*fs
+errpreset=conservative harmonicbalance=no
```

  - `fund` is the sampling frequency
  - `maxacfreq` is the highest frequency from which folding noise is relevant. Run several circuit simulations, doubling the value each time until the result no longer changes.

- Now perform the ac analysis:

```
pac1 pac start=1k stop=10G log=100
```

Advanced Analog Integrated Circuits

Sampling Noise

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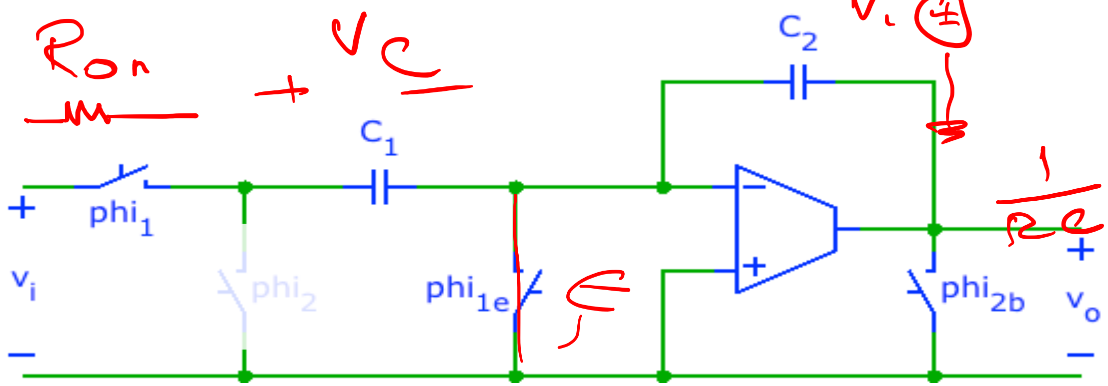
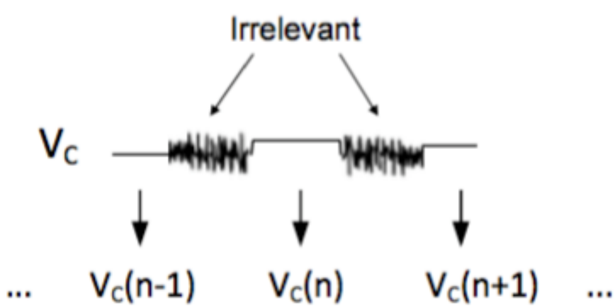
Sampling Noise

Noise in phase 1 (sampling phase):



$\frac{1}{RC} = \tau \ll \frac{T_s}{2} = \frac{1}{2 f_s}$

Voltage across C_1:

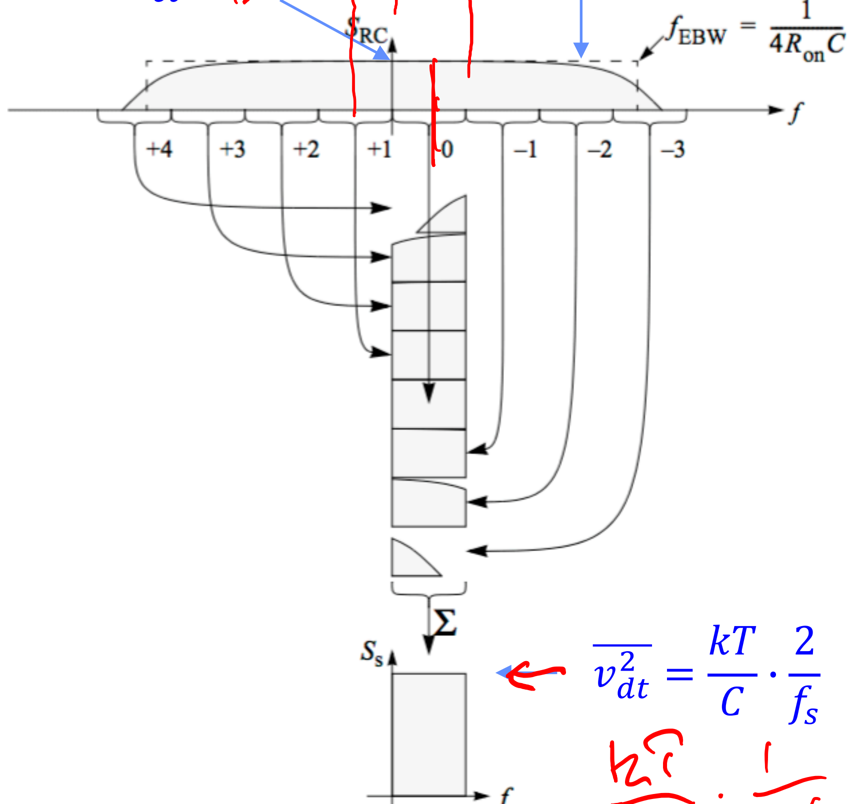


Ref: B. Murmann, *Thermal noise in track-and-hold circuits: Analysis and simulation techniques*, IEEE Solid-State Circuits Magazine, vol. 4, issue 2, Spring 2012, pp. 46-54.

Noise Folding

$-\frac{f_s}{2}$ $\qquad N = \frac{T_s}{\tau} = \frac{1}{f_s RC}$

$\overline{v_{ct}^2} = 4kTR$ $\quad f_{-3dB} = \frac{1}{2\pi RC}$



$\overline{v_{dt}^2} = \frac{kT}{C} \cdot \frac{2}{f_s}$

$\frac{kT}{C} \cdot \frac{1}{f_s/2}$

1 - sided $\quad f_{-3dB} = \frac{1}{2\pi RC}$

Noise densities:

Continuous time $\quad \overline{v_{ct}^2} = 4kTR$

Δf

Discrete time $\quad \overline{v_{dt}^2} = \frac{kT}{C} \cdot \frac{2}{f_s}$

Δf

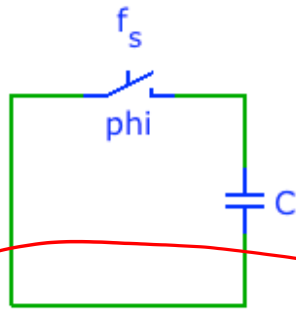
Ratio: $\quad \frac{\overline{v_{dt}^2}}{\overline{v_{ct}^2}} = \pi \frac{f_{-3dB}}{f_s} \gg 1$

$= \frac{kT}{C} \cdot \frac{2}{f_s} \cdot \frac{1}{4kTR} = \frac{1}{2f_s \cdot RC} =$

$= \frac{N}{2}$

Ken Kundert, http://www.designers-guide.org/analysis/sc-filters.pdf

Sampled RC Noise Spectrum



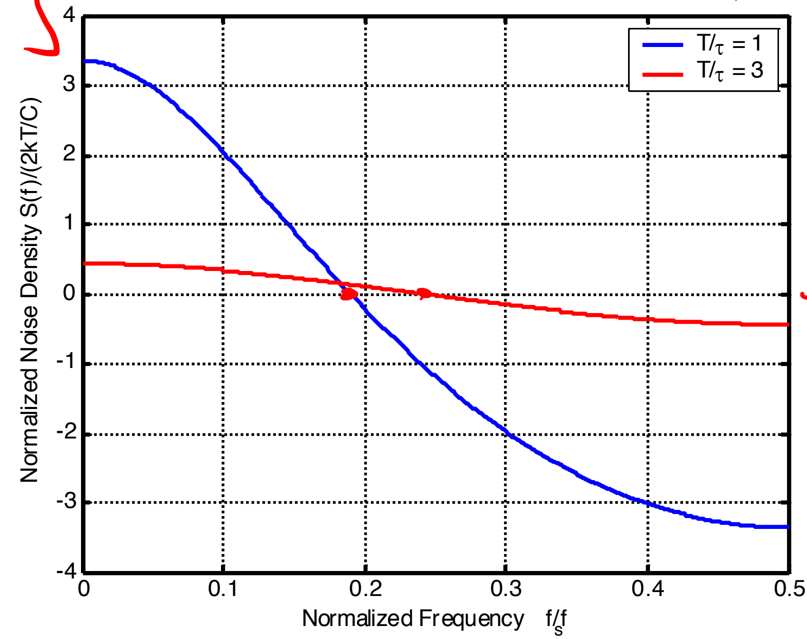
$$S_y(f) = \frac{k_B T_r}{C} \frac{2}{f_s} \frac{1 - e^{-2a}}{1 + e^{-2a}\left(1 - \cos 2\pi f T\right)}$$

$$a = \frac{T}{R_{sw} C} = \frac{\mathrm{T}}{\tau} \qquad \text{and} \qquad T = \frac{1}{f_s}$$

$$\int_0^{f_s/2} S_y(f)\,df = \frac{k_B T_r}{C}$$

N

[dB]



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Effective Noise Bandwidth

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SC Noise Analysis

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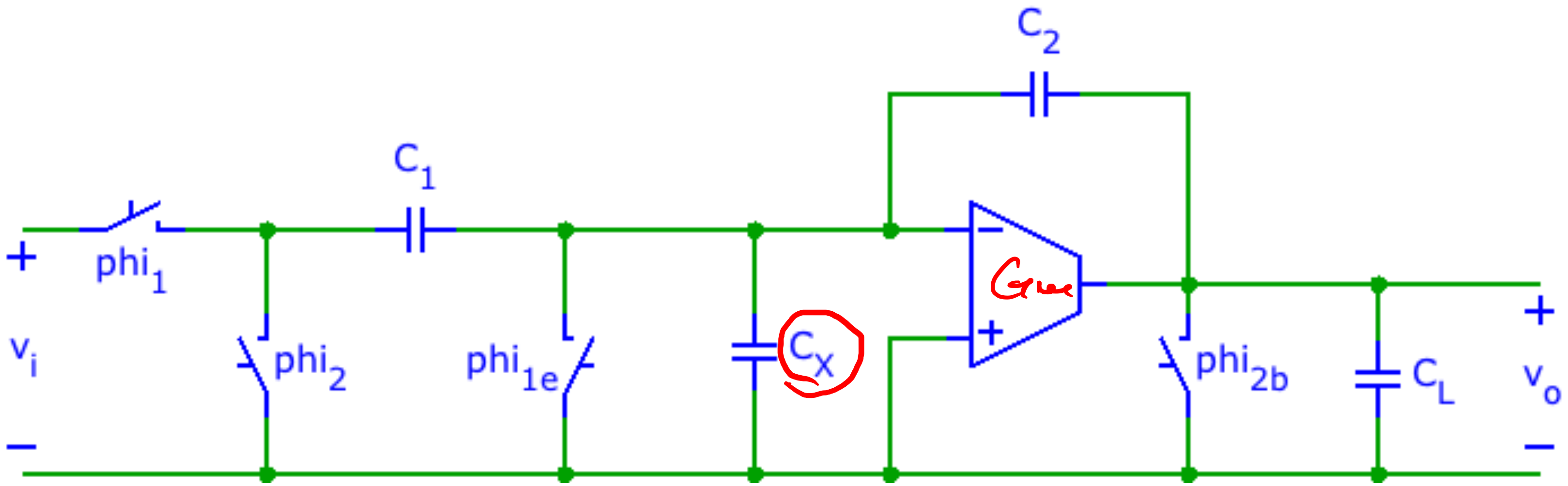
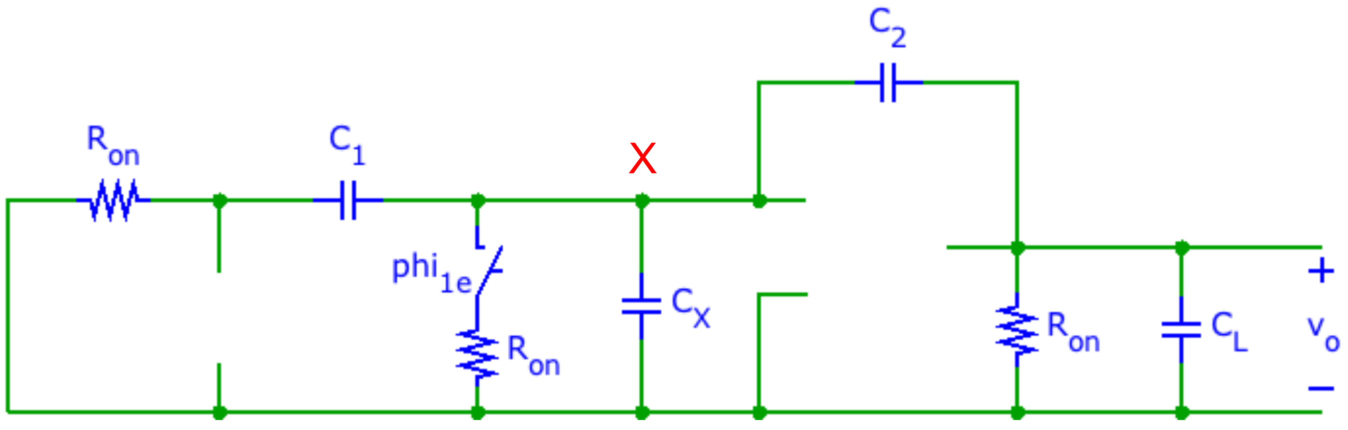
Circuit for Noise Analysis



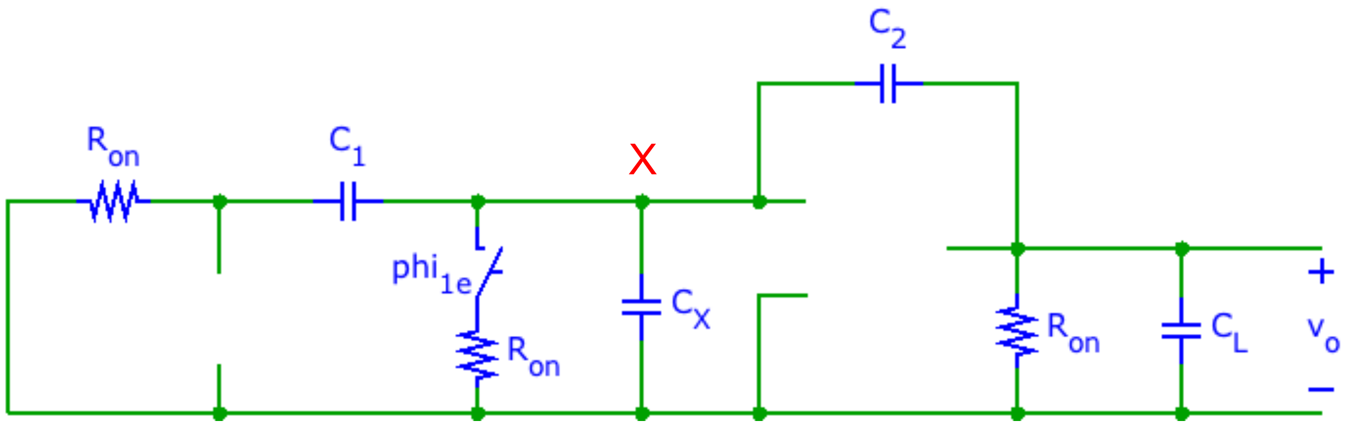
Assumptions:

- $R_{on} << 1/g_m$, $R_{off} \to \infty$
- OTA, th. noise
-

Noise in Phase 1



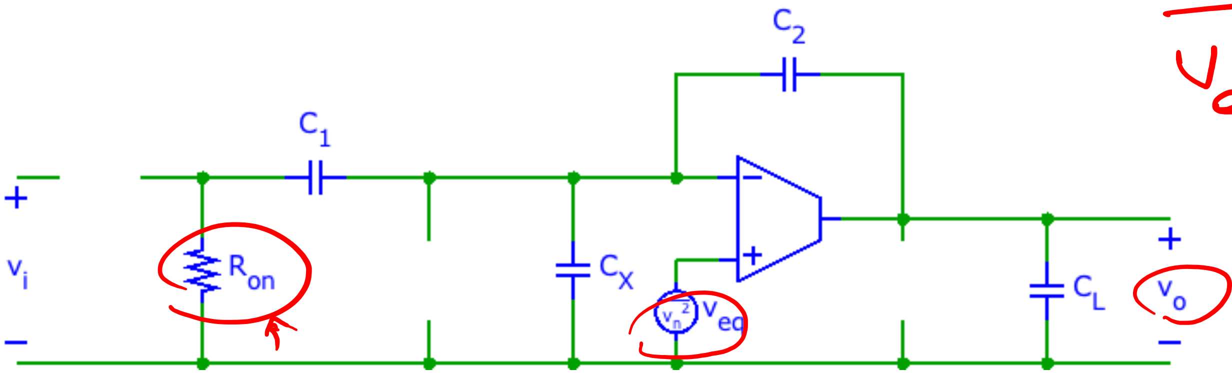
Equipartition Principle



$$\underbrace{\frac{1}{2}\frac{Q^2}{C}}_{} = \frac{1}{2} C V^2 = \underbrace{\frac{1}{2} k_B T}_{}$$

$$\overline{q_x^2} = kT \cdot \left(C_1 + C_2 + C_x\right)$$

Noise in Phase 2



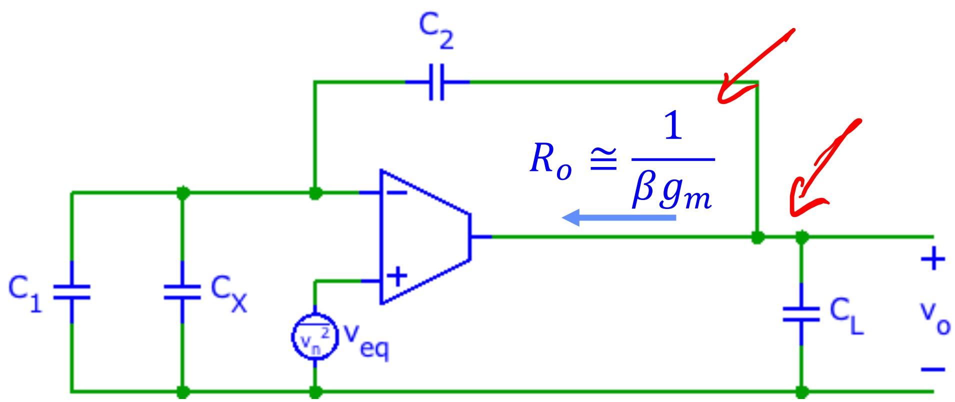
$$\overline{V_{eq}^2} = 4kT\frac{\alpha \cdot f}{g_m} \cdot \Delta f$$

- $\cancel{R_{on}}$ $\quad N_{sw} = 4kT \cdot R_{on} \cdot \Delta f \left(\frac{C_1}{C_2}\right)^2 \left|H(j\omega)\right|^2$

- Amp: $\rightarrow N_a = 4kT \frac{\alpha f}{g_m} \cdot \Delta f \cdot \left(1 + \frac{C_1}{C_2}\right)^2 \left|H(j\omega)\right|^2$

$$\frac{N_a}{N_{sw}} = \frac{\alpha f}{g_m \cdot R_{on}} \cdot \frac{\left(1 + \frac{C_1}{C_2}\right)^2}{\left(\frac{C_1}{C_2}\right)^2}$$

Total Integrated Amplifier Noise



$$\beta = \frac{C_2}{C_1 + C_2 + C_x}$$

$$C_{Ltot} = C_L + (1-\beta)\cdot C_2$$

$$BW = \frac{1}{R_o C_{Ltot}} = \frac{\beta \cdot g_m}{C_{Ltot}}$$

$$\overline{v_{oa}^2} = 4kT\frac{\alpha_f}{g_m}\cdot\frac{1}{\beta^2}\cdot\frac{BW}{4} = \boxed{\frac{\alpha_f}{\beta}\cdot\frac{kT}{C_{tot}}}$$

Total Noise from Phases 1 & 2

$$\overline{v_{\phi_1}^2} = \frac{\overline{q_x^2}}{C_2^2} = \frac{kT}{C_2}\cdot\underbrace{\frac{C_1+C_2+C_x}{C_2}}_{1/\beta} = \frac{kT}{\beta\cdot C_2}$$

$$\overline{v_{\phi_2}^2} = \frac{\alpha\gamma}{\beta}\cdot\frac{kT}{C_{Ltot}}$$

$$\boxed{\overline{v_{oT}^2} = \frac{kT}{\beta}\left(\frac{1}{C_2}+\frac{\alpha\gamma}{C_{Ltot}}\right)}$$

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Noise Simulation

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Methods to Simulate Noise for Verification

1. .noise analysis
   - Linear time-invariant circuits only
   - For time variant circuits, simulate each phase separately and combine results manually (as in hand analysis)

2. Periodic noise analysis
   - Analog to pac
   - Perform pss analysis first

   pnoise

3. Transient noise analysis
   - Closest to “reality”, very general
   - Average results from many simulations
   - Good alternative when pss has convergence problems
   - Can be slow …

Refs: B. Murmann, *Thermal noise in track-and-hold circuits: Analysis and simulation techniques*, IEEE Solid-State Circuits Magazine, vol. 4, issue 2, Spring 2012, pp. 46-54.

Ken Kundert, *Simulating Switched-Capacitor Filters with SpectreRF*, http://www.designers-guide.org/analysis/sc-filters.pdf

Periodic Noise Simulation (Spectre)

- Perform first a "periodic operating point analysis"
- Then perform the pnoise analysis:

```
pnoise1 pnoise (vo 0) fund=fs start=0 stop=fs/2
+noisetype=timedomain maxsideband=150
+noisetimepoints=[ 1us ]
```

  - `noisetype=timedomain` instructs the simulator to compute the spectrum of discrete time noise samples at specified sampling instances
  - `maxsideband=150` sets the maximum frequency relative to `fs` for which noise folding is significant. Try doubling this value and increase until simulator output converges.
  - `noisetimepoints=[ 1us ]` is the sampling instance. For the SC gain stage, this is near the end of phase 2
  - See simulator docs and http://www.designers-guide.org/analysis/sc-filters.pdf